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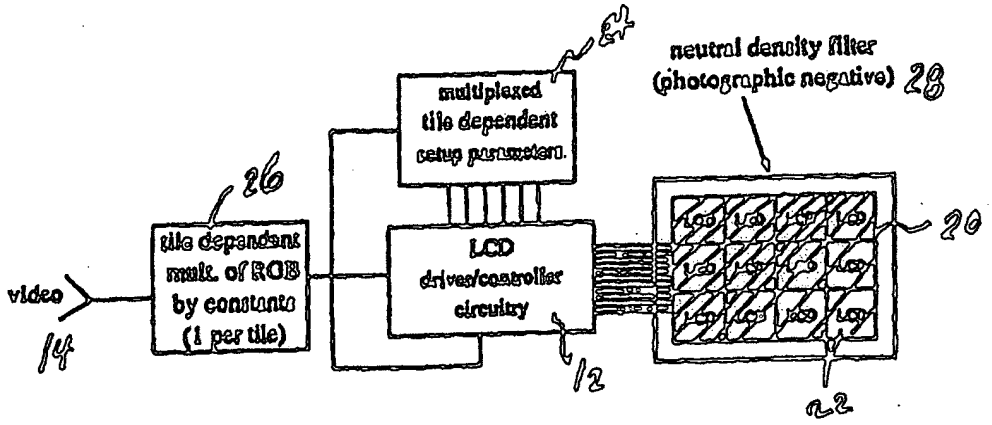

(57) Abstract

The present invention features a tiled, flat-panel, color display (20) that has a color-correction capability (24). The display is a tiled mosaic of individual display tiles (22), such as AMLCDs. Column and row inputs that are typically provided for a single display tile system are distributed over a plurality of display tiles. The color purity is achieved for the display by sorting the tiles into groups, matching their color coordinates, and correcting non-uniformities optically (e.g., by using a graded neutral density filter (28) having a grading function being the inverse of the brightness distribution non-uniformities) and/or electronically. Then, each individual tile in the mosaic is color-corrected via a multiplexed controller/driver circuit (12).

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TILED, FLAT-PANEL DISPLAYS WITH COLOR-CORRECTION CAPABILITY

Field of the Invention:

The invention pertains to flat-panel electronic displays and, more particularly, to a flat-panel, electronic display with color-correction capability, a display that is assembled by piecing together a plurality of matched color tiles.

BACKGROUND OF THE INVENTION

Images on electronic displays are derived from an array of small picture elements known as pixels. In color displays, these pixels comprise three color elements that produce the primary colors red, blue and green. Usually arranged as squares or rectangles, these pixels can be characterized by pixel pitch, P, a quantity that measures the density of pixels per unit distance. A typical cathode-ray tube has a pixel pitch of 0.3 mm. Typical small computer screens have a width:height ratio of 4:3. Pixel arrays are typically disposed in a 640 x 480 or 1024 x 768 configuration.

Large displays comprise a plurality of adjacent tiles having a single pixel or an array of pixels. The tiles are characterized by visually disturbing seams, resulting from gaps between adjacent pixels on the same and/or adjacent tiles. The image portrayed by utilizing a seamed panel appears segmented and disjointed. Therefore, it is

desirable to fabricate a tiled, flat-panel display which does not have noticeable or perceptible seams.

The pixel pitch in electronic displays is set so that the minimum viewing distance will produce an imperceptible seam. With a pixel pitch P = 0.3 mm, the minimum viewing distance is on the order of one meter. The minimum viewing distance will increase with the pixel pitch; therefore, when designing for the purpose of visually eliminating the seams, there is very little latitude in selecting the pixel pitch.

Flat-panel displays include liquid crystal displays (LCDs), active matrix LCDs (AMLCDs), plasma displays (PDs), field emission displays (FEDs), electroluminescent displays (ELDs) and digital mirror displays (DMDs), all of which depend on the microfabrication of the key components carrying the pixel patterns. AMLCD is a technology curently favored by the industry. For purposes of clarity, the term "LCD" is used herein, but is intended to describe all flat-panel displays. From a practical point of view, the microfabrication yield is unacceptable for large displays, due to the unacceptable number of manufacturing rejections. The inventors, therefore, have determined that small pixel arrays (tiles) can be microfabricated and, after appropriate selection, then assembled together to form a larger display configuration. However, past attempts to accomplish this have led to visible seams, due, in large part, to the dimensions required by tile assembling, which goes beyond even the pixel spacing required of monolithic displays. This is essentially why few attempts have been made to achieve

large, color, "seamless", tiled panels.

In co-pending U. S. patent applications, Serial Nos. 08/593,759 and 08/571,208, which were filed on January 29, 1996, and December 12, 1995, respectively, a method of constructing a seamless, tiled, flat-panel display is illustrated. The teachings of these companion applications are meant to be incorporated herein by way of reference.

The electronic circuitry associated with a non-tiled display has two functions:

(1) translate the incoming electronic representation (video signal) of the image to be displayed into a format compatible with the display device, and send this tranformed signal continuously and in real time to the display device; and

(2) provide set-up and adjustment capability to the display. Brightness, contrast, threshold, tint, white point and reference levels are examples. Some of these adjustments can be set by both the viewer and the display manufacturer; others are not viewer-accessible. To the display manufacturer, these adjustments allow reasonable manufacturing tolerances. They also allow for variations across the viewing area of each individual display unit that occur, at least in part, due to an inherent variability in manufacturing processes. These permit the viewer to perceive a more acceptable picture quality. To the viewer, these adjustments allow some picture quality attributes to be changed, in order to suit individual preferences.

The extension of the first function to a tiled display is straightforward. This invention describes methods of extending the second function to a tiled display in such a way so that the picture quality is equivalent to a non-tiled display. Alternative methods of improving the picture quality of a tiled display and making it visually comparable or superior to that of a non-tiled display are based on new techniques for the aforementioned function (1) and combinations of functions (1) and (2).

The present invention provides unique circuitry and a tile assembly for achieving color purity in a "seamless" tiled display, comprising a tiled mosaic of individual LCDs. In a commercially acceptable tiled display, the color purity has to be uniform for each tile. That is, there should be no apparent differences in brightness or color between tiles over the entire range of input video signals to be rendered.

The optical performance of the display can be characterized by parameters that describe the voltage input to picture elements (pixels) and the resulting transmission of the elements. For example, AMLCDs have threshold voltages V_{TH} and V_{Dmax} for maximum and minimum transmission, T_{max} and T_{min} (see FIGURE 1aa). The pixel optical gain, V_{SL}, can be described as the slope of the transmission-voltage curve. Color coordinates may also vary. A similar set of parameters can be identified for other types of flat-panel displays.

In the extension to tiled displays, additional

parameters related to the quality of the display near the edge can be identified, for example, due to the filling of the liquid crystal material. Other optical components of the display may also vary.

Color purity is defined as the condition of uniform saturation of primary colors over the screen. There are several sources of inter-tile color differences, including differences in the color coordinates between tiles, threshold and transmission voltages in the pixels adjacent the seams, etc.

The inventors realize that individual tiles can provide acceptable color purity; therefore, a standard LCD controller/driver chip set, as is commercially available from Toshiba or Hitachi, can be integrated into a circuit for achieving total color purity throughout a tiled LCD display.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a tiled, flat-panel display with color-correction capability. The display comprises a tiled mosaic of individual LCDs. Column and row inputs that are typically provided for a single LCD system are distributed over a plurality of LCD tiles. The color purity is achieved for the display by sorting the tiles into groups of individual LCDs on the basis of their color coordinates prior to assembly. Obtaining a matched set is defined as having the intra-tile average color coordinate values for each

primary color (e.g., red, green and blue) to fall within a specified range for each tile. Each individual tile in the mosaic has its own set of parameters for the controller/driver circuit. The sets of such parameter values are multiplexed at the correct times to the controller, so that appropriate values will be present, when data is being written to each tile. Average tile brightness is achieved by scaling the video level with a tile-dependent set of constants (one for each tile). Discontinuities, or large level shifts from one tile edge to another, are corrected for by placing a negative of the display (i.e., a graded neutral density filter, in the preferred embodiment) on the screen. This will match the brightness levels across the entire display. The exposure will be made so that the dimmest region has no reduction; only the brighter regions will be reduced. This discontinuity correction can also be accomplished by adjusting (balancing) signals electronically.

It is an object of this invention to provide an improved flat-panel, tiled, color display.

It is another object of this invention to provide a flat-panel, tiled, color display that is constructed with matched, color-coordinated tiles.

It is a further object of the invention to provide a color-correcting circuit for a tiled, color display.

BRIEF DESCRIPTION OF THE DRAWINGS

A complete understanding of the present invention may be obtained by reference to the accompanying drawings, when considered in conjunction with the subsequent detailed description, in which:

FIGURE 1aa is a transmission versus voltage curve for a normally white liquid crystal cell;

FIGURE 1a shows a schematic plan view of the column (data) and row (control) inputs for a typical, single LCD array;

FIGURE 1 depicts a schematic plan view of the column and row inputs for a tiled LCD system;

FIGURE 2 illustrates a schematic view of a controller/driver circuit for the single LCD shown in FIGURE 1;

FIGURE 3 depicts a schematic view of a controller/driver circuit as applied to a tiled LCD system having intra-tile color purity;

FIGURE 4 illustrates a schematic diagram of the circuit of FIGURE 3 with further correction for average tile brightness;

FIGURE 5 shows a schematic diagram of the circuit of FIGURE 4 with additional correction for discontinuities between tile edges;

FIGURE 6 shows a schematic diagram of an alternate embodiment of a circuit for multiplexing set-up parameters to tile driver circuitry;

FIGURE 7 is a cross-sectional view of a typical, tiled flat-panel display that incorporates a single color-balancing filter;

FIGURE 8 is a cross-sectional view of a typical flat-panel display wherein each tile incorporates a separate color-balancing filter;

FIGURE 9a is a top view of a typical, flat-panel display showing reference points corresponding to the relative transmission plot shown in FIGURE 9b;

FIGURE 9b shows the relative light transmission of a typical, tiled flat-panel display under average white-field drive conditions, both with and without a color-balancing filter; and

FIGURE 10 is a system block diagram showing typical components that are required to display a video image on an LCD display.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally speaking, the present invention features a tiled, flat-panel, color display that has a color purity correction capability. The display comprises a tiled mosaic of individual LCDs. Column and row inputs that are typically provided for a single LCD system are distributed over a predetermined number of LCD tiles. The color purity is achieved for the display by sorting the tiles into groups of individual LCDs, based on their color coordinates, prior to assembly. Then, each individual tile in the mosaic is color-corrected via a multiplexed, controller/driver circuit.

Now referring to FIGURE 1a, a schematic plan view of the column "Q" and row "P" inputs for a typical, single LCD array 10 is illustrated. The display 20 of this invention is constructed of a plurality of individual LCD tiles, having inputs Q and P that are fed to each LCD tile, as illustrated in FIGURE 1. The tiles are sorted into groups of individual LCD tiles for a given display assembly, each of which is matched with the same color coordinates prior to assembly. Having a matched set is defined as an LCD display wherein each tile has inter-tile average values that are within a specified range of each other, and which do not exceed a given or specified value. Sorting may be performed in a variety of ways, depending upon the type of flat-panel tile being used. For example, for AMLCDs, the sorting may be performed on the tile top pieces (color filter array), before or after the bottom piece thin film transistor (TFT) is attached. In co-pending U. S. patent application, Serial No. _____,

adjustments for pixel level non-uniformities and backlight are discussed.

Referring to FIGURE 2, a schematic view of a controller/driver circuit is shown for the single LCD display 10 illustrated in FIGURE 1a. Such systems use commercial, LCD controller/driver chip sets 12. The video signal 14 is fed to the LCD driver/controller circuitry 12, which, in turn, controls the LCD 10. The inter-tile color correction must be made compatible with the functionality of, and connect to, the existing input pins of the chip set. By adjusting the set-up parameters 16, acceptable picture quality can be achieved.

Referring to FIGURE 3, a schematic is shown for the tiled LCD display 20 illustrated in FIGURE 1. Each individual tile 22 in the mosaic has acceptable color purity with its own set of parameters for the controller/driver circuitry 12. The parameter values may be multiplexed (block 24) at the correct times to the controller, so that the appropriate values will be present when the data is being written to each tile 22.

Referring to FIGURE 4, the video signal 14 is now adjusted (block 26) with a tile-dependent set of constants (one for each tile 22), in order to match the average tile brightness for each of the tiles.

Referring to FIGURE 5, the discontinuities, or large level shifts between the edges of each tile 22, are nullified by making a negative (a graded neutral density filter having a gradient which is the inverse of the color

non-uniformities) 28 of display 20, and placing it over the screen (not shown) of the display 20. This negative 28 can also be printed on the screen's front polarizer (not shown), or a separate thin plastic sheet (not shown). This will match the brightness levels across the entire surface of the display 20. The exposure will be made so that the dimmest region has no reduction. Only the brighter regions will be reduced. It is also possible to accomplish this electronically with another level of tile-dependent balancing parameters having a finer mesh (similar to those of block 26).

Referring now to FIGURE 6, there is shown a block diagram of an alternate method for applying tile-dependent correction constants to each of a plurality of tiles in a flat-panel display. A video signal 30 is applied to a commercially available LCD controller 32. An output signal 34 from LCD controller 32 is applied simultaneously to each of a plurality of drivers 36, with each driver 36 being associated with an individual display panel 38. Each driver 36 is adapted to receive individual correction constants from parameters 40, which were previously stored in a memory device (not shown). Alternatively, set-up parameters may be permanently connected to the driver circuitry for each tile. In such case, a common controller can still be used, as illustrated in FIGURE 6. Individual, predetermined correction constants 40 are permanently provided to individual tile drivers 36 in this arrangement.

Referring now to FIGURE 7, there is shown generally at reference number 50, a cross-sectional view of the

structure of a typical, tiled, flat-panel display, used in the preferred embodiment. It should be understood, however, that components can be disposed in other sequences without departing from the scope of this invention. A color-balancing neutral density filter 52 is disposed at the top of the display structure 50. Immediately below filter layer 52 is a top optics layer 54. This optics layer 54 may contain a mask, screen, micro-lens or polarizer components, as described in the aforementioned, co-pending U. S. patent application Serial No. 08/593,759. Disposed below the optics layer 54 is an optional, color-correcting neutral density filter 52'. Color-correcting filter 52' could replace color-balancing filter 52 or could be employed in addition thereto. Beneath the optional color-correcting filter 52' is a plurality of individual tiles 56. In the preferred embodiment, tiles 56 are AMLCD tiles, with or without top and/or bottom polarizers.

Directly below tiles 56 is a third color-correcting neutral density filter 52'', also optional. As indicated with filters 52 and 52', color-correcting filter 52'' could either replace or augment any combination of filters 52 and 52'. Below the optional filter 52'' is a bottom optics layer 58. This bottom optics layer 58 may contain a mask, screen, micro-lens or polarizer components, as also described in detail in co-pending U. S. patent applications, Serial Nos. 08/593,759 and 08/571,208. The bottom layer of the flat-panel display 50 is a light source 60.

Referring now to FIGURE 8, there is shown generally at

reference number 70 a cross-sectional view of another embodiment of a tiled, flat-panel display. This embodiment differs from the tiled, flat-panel display 50 (FIGURE 7), in that discrete, color-correcting neutral density filter layers 52' and/or 52'' are associated with the respective individual tiles 56. That is, each individual tile 56 has associated with it a unique filter layer 52' and/or 52''. In the tiled, flat-panel display 50 (FIGURE 7), on the other hand, a single filter layer 52, 52', or 52'' covers more than one tile 56 and possibly an entire matrix of tiles.

Referring now to FIGURE 9a, there is shown a plan view of the top surface of a typical, tiled, flat-panel display 80. Locations A (82), B (84) and C (86) are points on the surface of display 80. These points 82, 84 and 86 are defined by x,y coordinates along the indicated x and y axes.

FIGURE 9b graphically depicts the relative optical transmission T 88 of a tiled, flat-panel display 80 (FIGURE 9a) under average, white-field drive conditions at y = C, from x = A to x = B. Two relative transmission curves 90 and 92 are plotted in dashed and solid lines, respectively. Transmission curve 90 depicts the actual relative optical transmission across three uncorrected tile segments 94, 94' and 94'' that are separated by tile boundaries 96 and 96', as shown. Particular attention should be paid to the abrupt discontinuities which occur at tile boundaries 96 and 96'. Transmission curve 92 shows a corrected, effectively "flat" transmission across the three tiles 94, 94' and 94''. The corrected, flat

transmission of curve 92 was achieved by the application of an appropriately graded, neutral density color-correction filter (not shown). Such a filter effectively compensates for relative transmission differences across individual tiles. The filter's effect becomes pronounced at the tile boundaries 96 and 96', where the abrupt discontinuities observed in curve 90 are eliminated.

Referring now to FIGURE 10, there is shown a block diagram interconnecting the components of a typical LCD display. A video signal (not shown) is first applied to a graphics controller 100. This graphics controller 100 retrieves digitized image information from memory (not shown) and generates both image data 102, and control and synchronization information 104. Graphics controllers are commercially available.

Image data signal 102, and the control and synchronization signal 104 are applied to the inputs of an LCD controller 106, which is typically implemented as an application-specific integrated circuit (ASIC). The function of the LCD controller 106 is to generate additional timing and control signals that are responsive to input signals 102 and 104, in order to control the row driver ICs 108 and column driver ICs 110. In addition, LCD controller 106 provides signals to other circuitry necessary for the operation of an LCD-type display. Reference voltage generator 112 provides a set of voltages (usually DC) necessary to match the unadjusted relative transmission of individual LCD tiles, as shown in curve 90 (FIGURE 9b), to the corrected relative transmission curve 92. These reference voltages are typically

generated by circuits, such as operational amplifiers, digital-to-analog converters or the like. The level of these reference voltages may be adjusted with any additional control circuitry (not shown) required by a specific application. For AMLCDs, row drivers 108 may be implemented as ICs, and generate gate voltage pulses that are typically in the 15 - 40 volt range to the gate of thin film transistors (not shown). Typical ICs suitable for use as column drivers are S-MOS SED1743 and Texas Instruments' type 57600 devices. Column drivers 110 generate the voltage signal levels representative of the input video signal (not shown). These voltages are provided to the sub-pixels by gate pulses. Column drivers 110 are generally implemented as ICs, with typical examples being Cirrus Logic CL-FP6522, Texas Instruments TMS 57481 and Vivid Semiconductor VS1192 devices.

It should be understood that other or ancillary control and video signal processing-circuitry can be used, depending on the type of tiles used to construct the flat-panel display.

Since other modifications and changes varied to fit particular operating requirements and environments will be apparent to those skilled in the art, the invention is not considered limited to the example chosen for purposes of disclosure, and covers all changes and modifications which do not constitute departures from the true spirit and scope of this invention.

Having thus described the invention, what is desired to be protected by Letters Patent is presented in the subsequently appended claims.

What is claimed is:

1. A tiled, substantially flat, panel display with color-correction capability, comprising:

a mosaic of individual display tiles of a given number, said display tiles having column and row inputs that are typically provided for a single display tile system, said column and row inputs being distributed over said given number of tiles, said display tiles being sorted into groups that have substantially matching color coordinates prior to assembly into a display, with each individual tile in the mosaic having its own set of characteristics;

means defining a video input signal; and

controller/driver means connected to said mosaic for selectively applying said video input signal to said mosaic, so that color purity is maintained.

2. The tiled, substantially flat, panel display with color-correction capability in accordance with claim 1, further comprising means for balancing said video input, wherein average tile brightness is achieved by modifying a level of said video input with a tile-dependent set of parameters.

3. The tiled, substantially flat, panel display with color-correction capability in accordance with claim 1, further comprising a graded neutral density filter, the grading function being the inverse of the brightness distribution non-uniformities in the display.

4. The tiled, substantially flat, panel display with color-correction capability in accordance with claim 3, wherein said inverse of the color non-uniformities in the display will substantially match the brightness levels across the entire display, and wherein the dimmest regions of the display have the least reduction.

5. The tiled, substantially flat, panel display with color-correction capability in accordance with claim 1, further comprising means for electronically modifying the video input, wherein brightness levels across the entire display will be substantially matched.

6. The tiled, substantially flat, panel display with color-correction capability in accordance with claim 1, wherein said mosaic is defined as a selected, substantially matched set of display tiles having the intra-tile average values of brightness and color for each color fall within a specified range for each display tile.

7. A seamless, tiled, substantially flat, panel display with color-correction capability, comprising:

a seamless mosaic of individual display tiles of a given number, said display tiles having column and row inputs that are typically provided for a single display tile system, said column and row inputs being distributed over said given number of tiles, with each individual tile in the mosaic having its own set of characteristics;

means defining a video input signal; and

controller/driver means connected to said mosaic for selectively applying said video input signal to said mosaic, so that color purity is maintained.

8. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 7, further comprising means for balancing said video input signal, wherein average tile brightness is achieved by modifying a level of said video input with a tile-dependent set of parameters.

9. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 7, further comprising a graded neutral density filter, having a grading function which is the inverse of the brightness distribution non-uniformities of said mosaic.

10. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 9, wherein said graded neutral density has a minimum optical density at the dimmest region of said display.

11. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 7, further comprising means for electronically modifying said video input signal, wherein brightness levels across the entire display will be substantially matched.

12. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 7, wherein said mosaic is defined as a selected, substantially matched set of display tiles having the intra-tile average values of brightness and color for each color fall within a specified range for each display tile.

13. The seamless, tiled, substantially flat, panel display with color-correction capability in accordance with claim 8, wherein said display tiles are LCDs and wherein said tile-dependent set of parameters that determine the display characteristics of each tile comprises any of the elements taken from the set of:

a) threshold voltage values of a pixel;
b) maximum/minimum transmissivities of a pixel;
c) pixel voltage optical gains;
d) color coordinates; and
e) tile edge-related parameters.

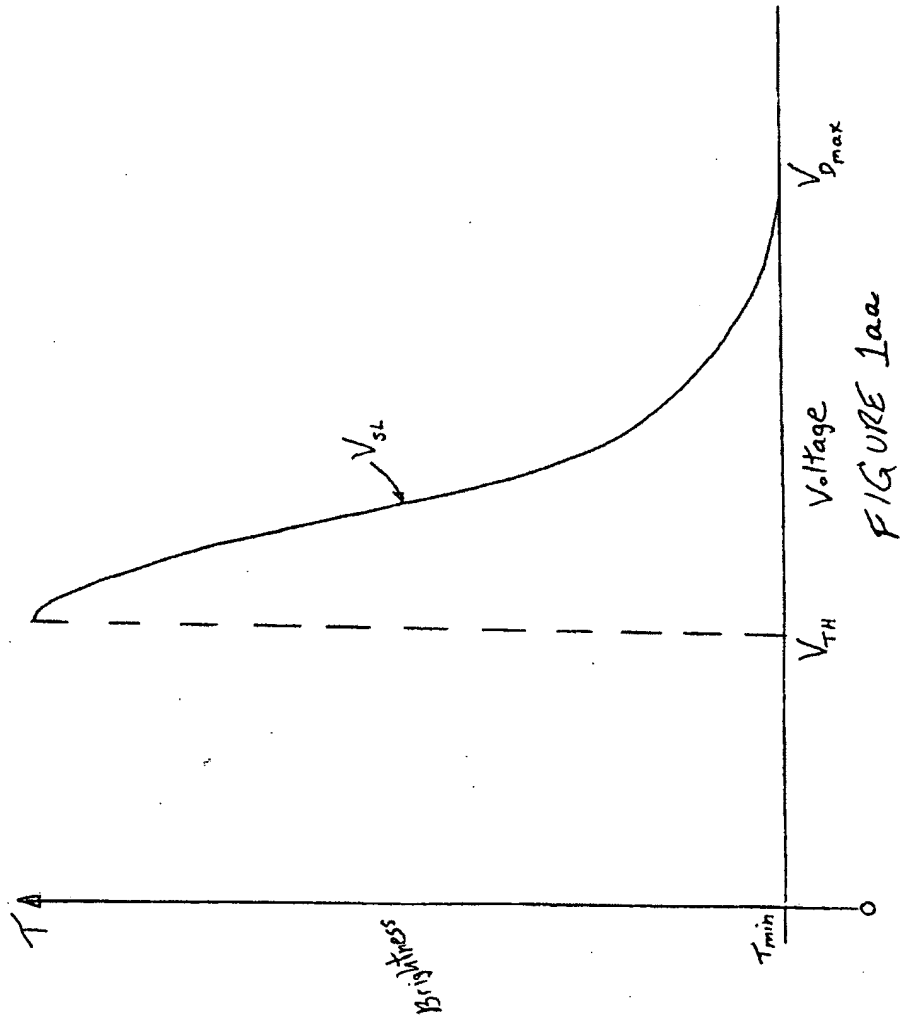

FIGURE 1aa

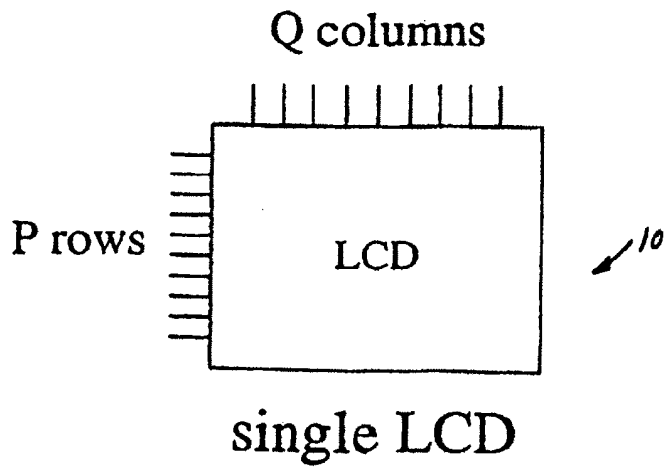

FIGURE 1a.

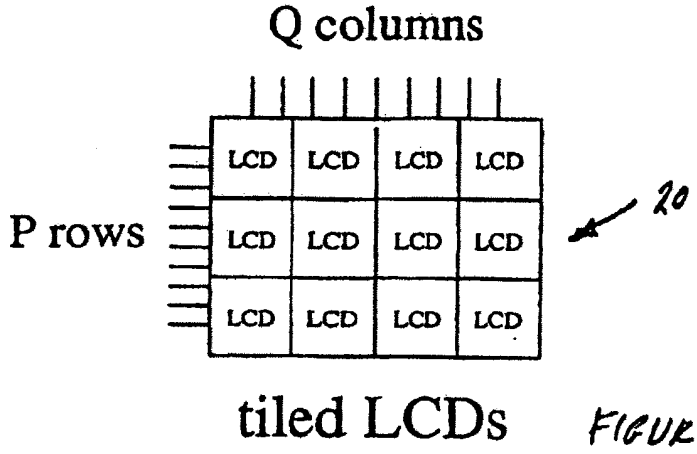

FIGURE 1

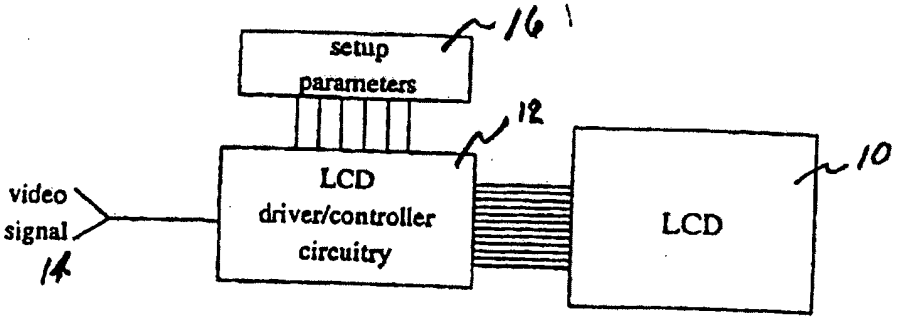

FIGURE 2

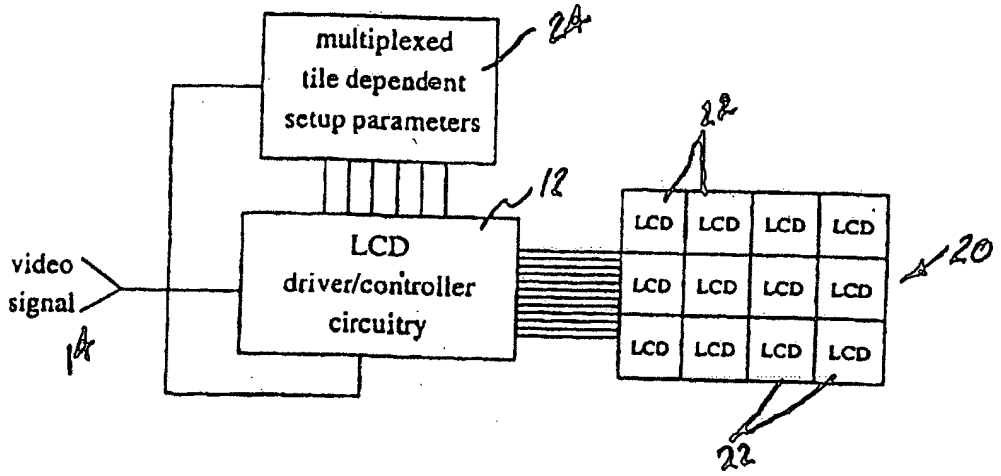

FIGURE 3

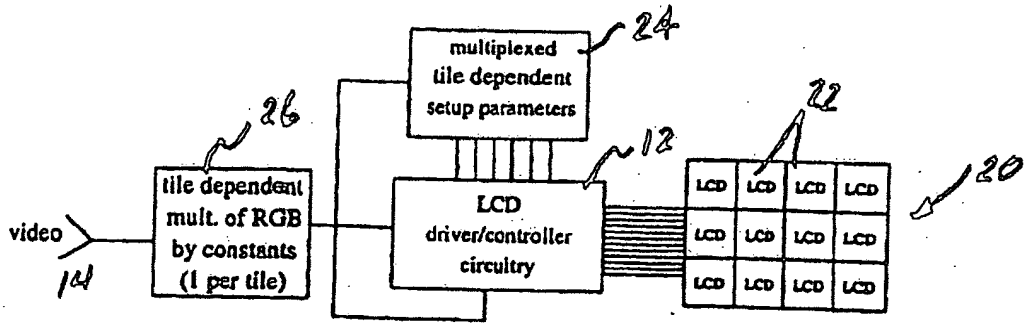

FIGURE 4

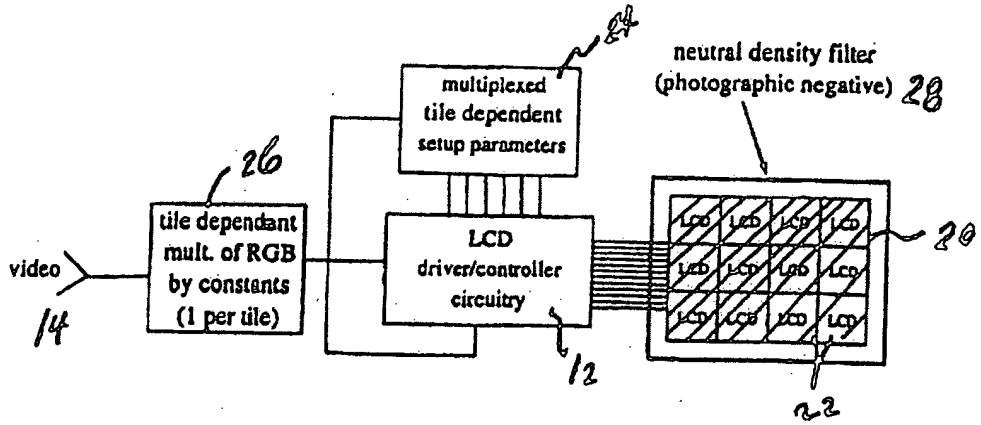

FIGURE 5

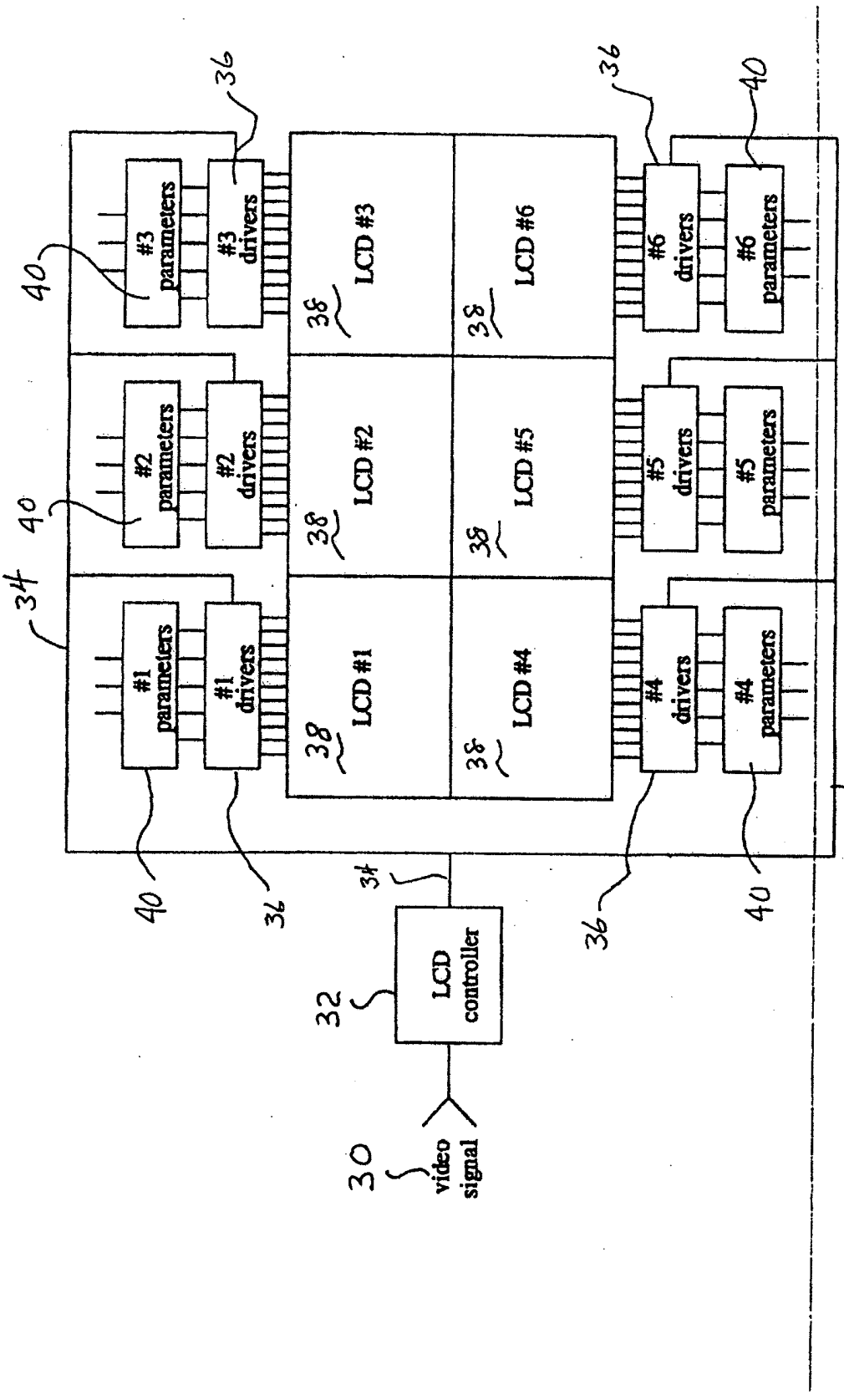
video signal
30
LCD controller
32
34
36
40
38
LCD #1
LCD #2
LCD #3
LCD #4
LCD #5
LCD #6
#1 drivers
#2 drivers
#3 drivers
#4 drivers
#5 drivers
#6 drivers
#1 parameters
#2 parameters
#3 parameters
#4 parameters
#5 parameters
#6 parameters

FIGURE 6

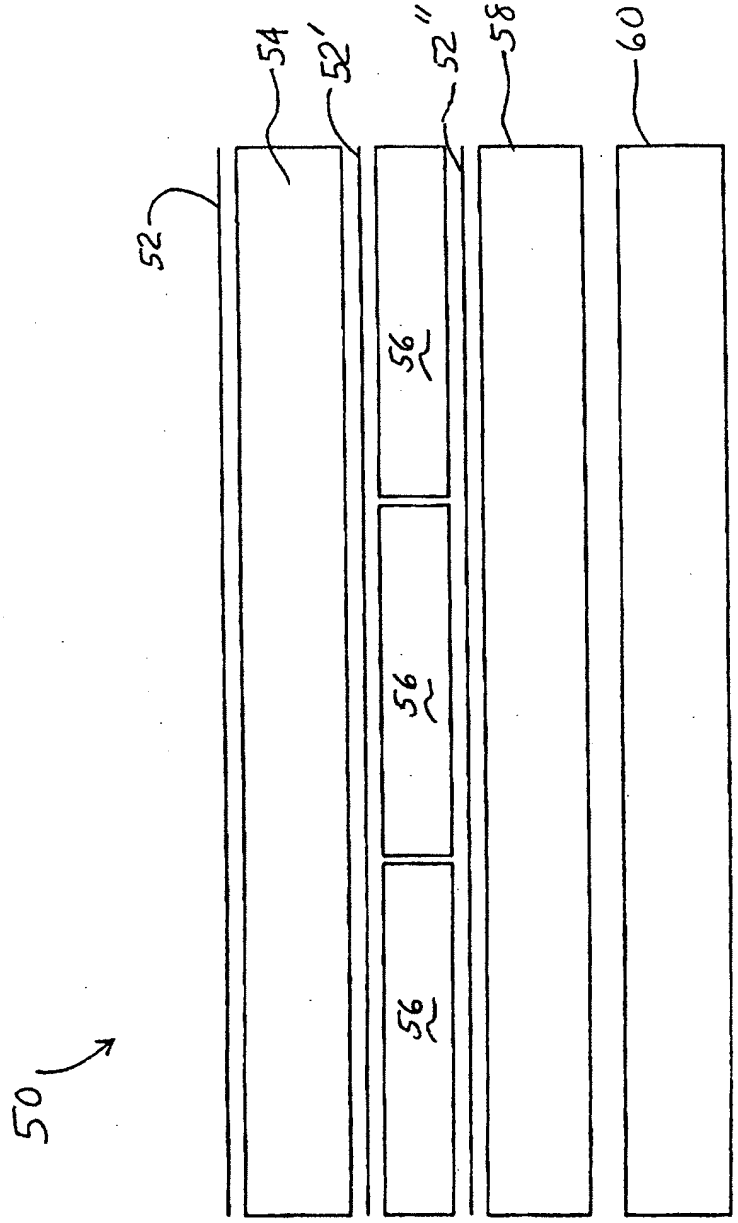

FIGURE 7

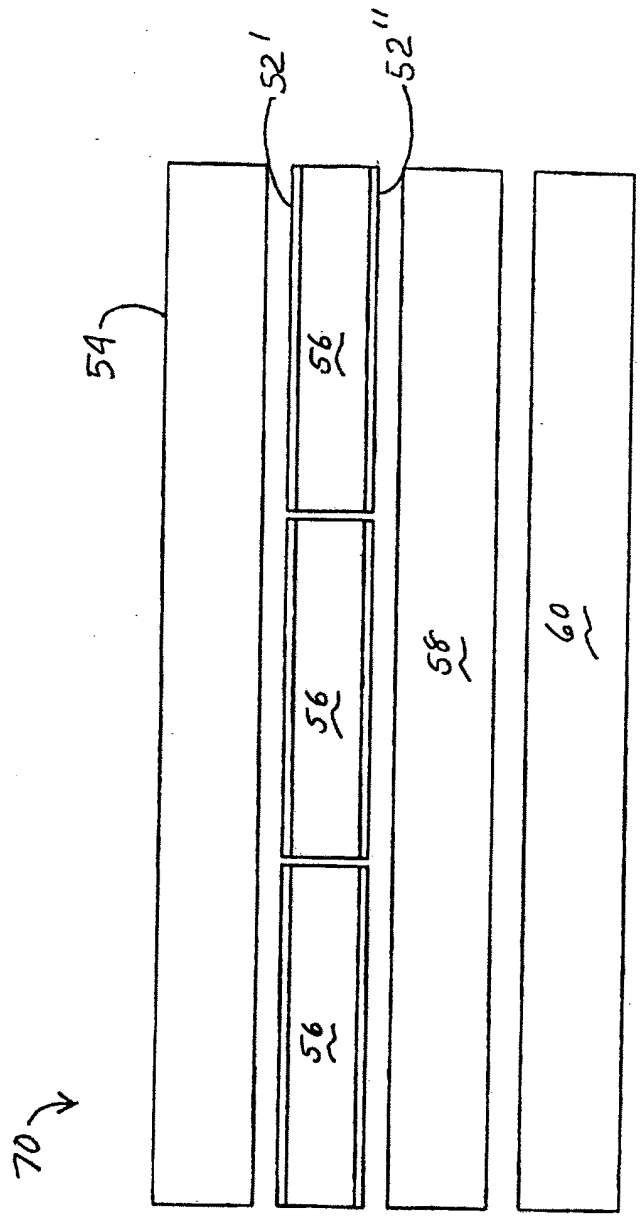

FIGURE 8

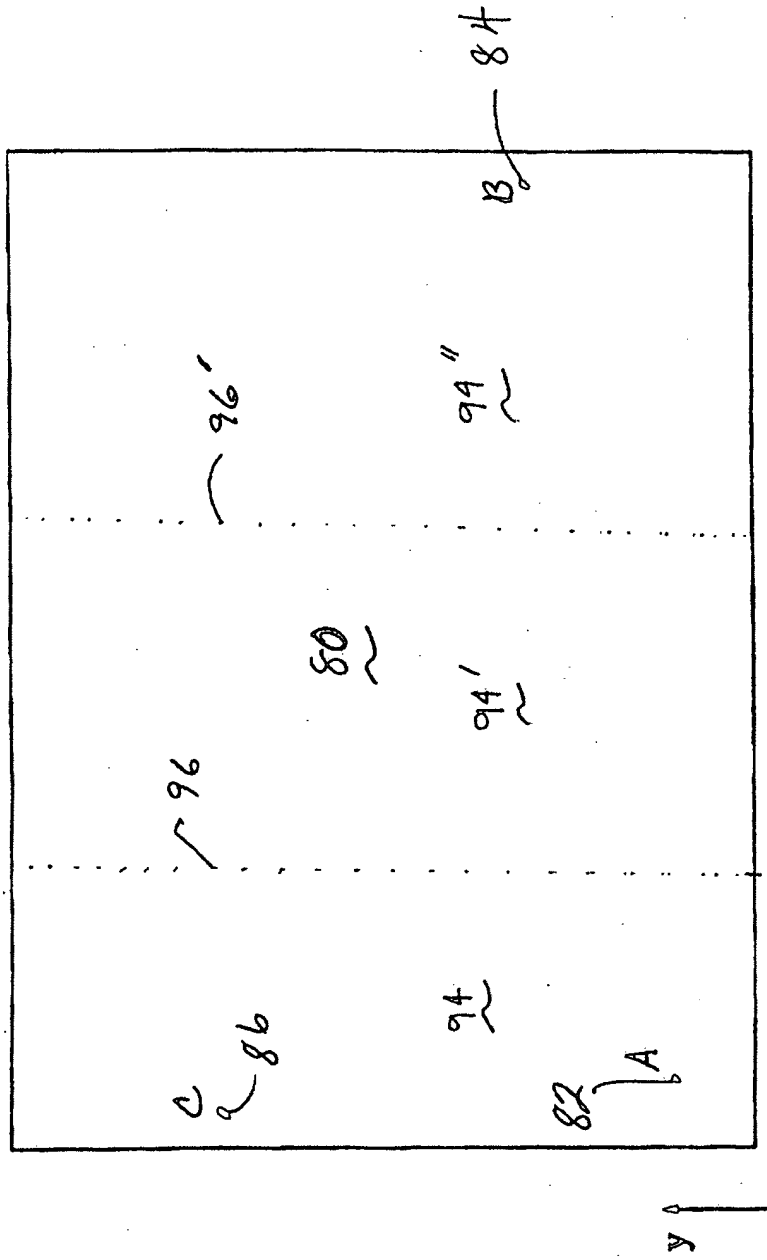

FIGURE 9a

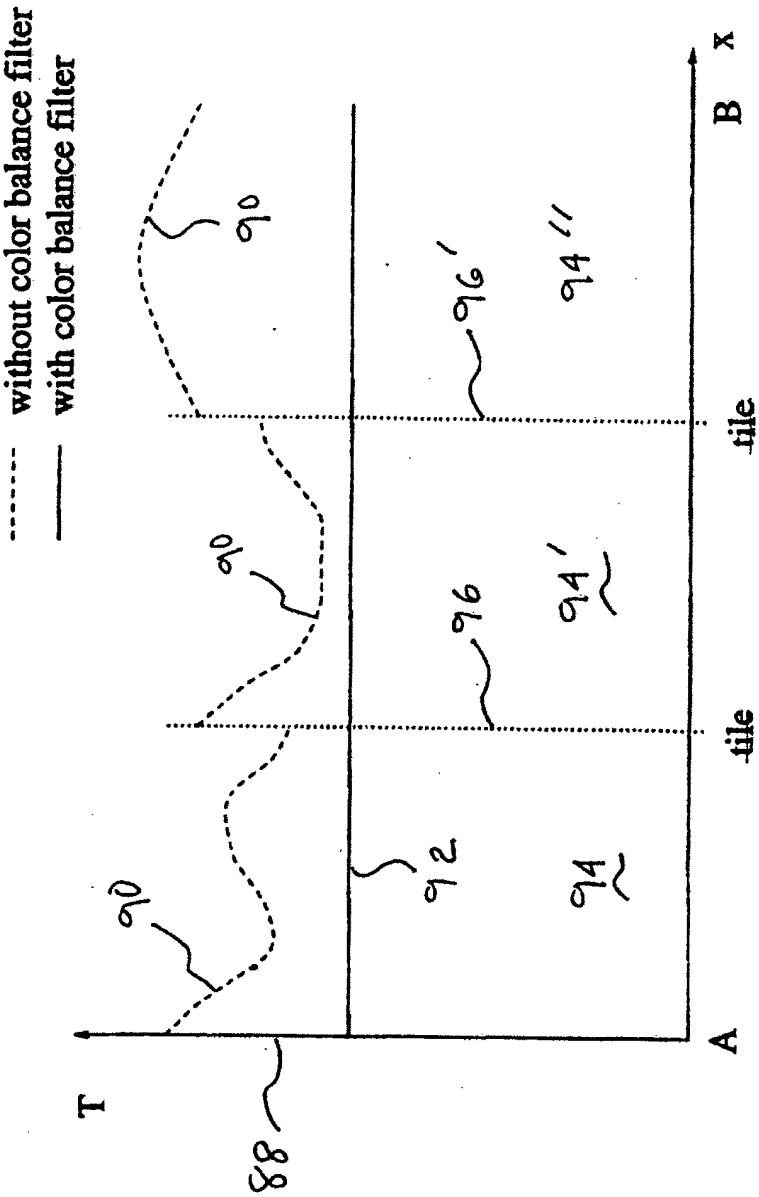
without color balance filter
with color balance filter
T
A
B
x
88
90
90
90
92
94
94'
94''
96
96'
tile boundary
tile boundary

FIGURE 9b

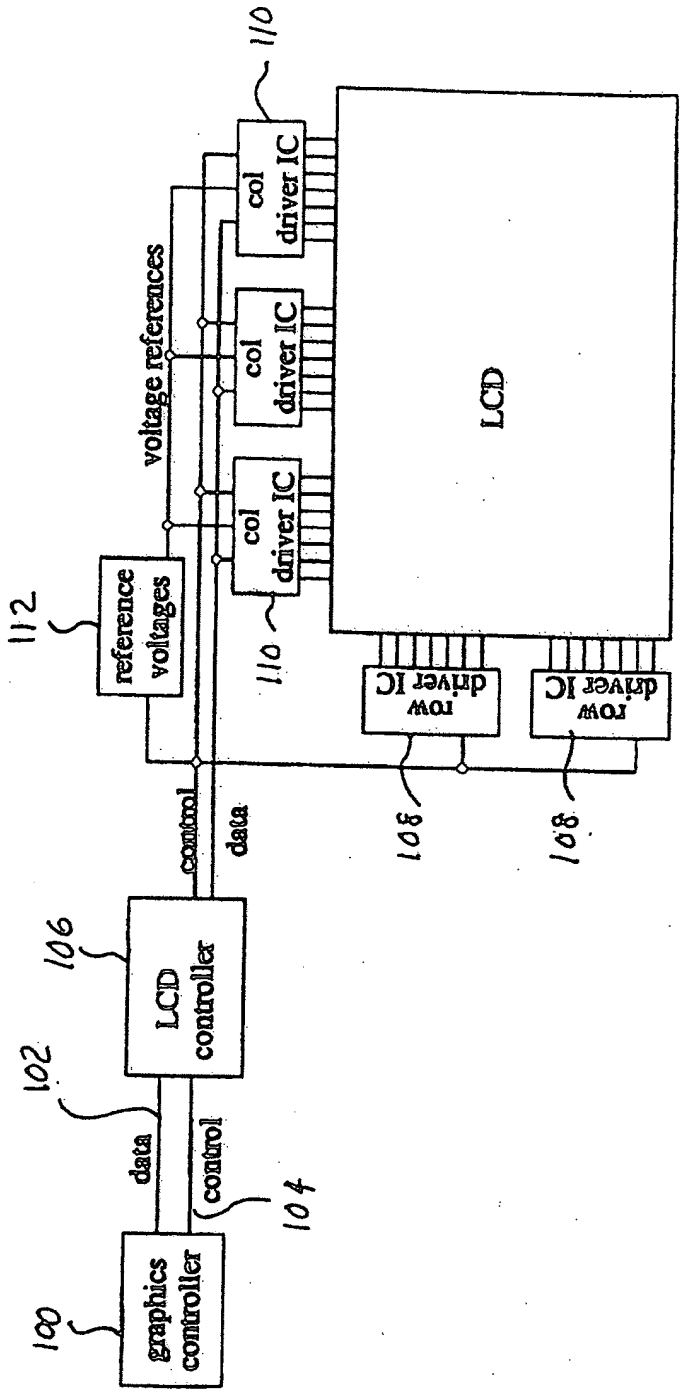
graphics controller
100
data
control
102
104
LCD controller
106
control
data
reference voltages
112
voltage references
col driver IC
col driver IC
col driver IC
110
110
LCD
row driver IC
row driver IC
108
108

FIGURE 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/04869

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G09G 5/00, 3/00, 3/36, 5/02, 5/04; H04N 5/66, 9/30; G02F 1/13
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/1, 32, 88, 90, 102, 103, 150, 152, 153; 348/383, 791; 349/106, 109, 112

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, MAYA
search terms: color correction, color coordinates, graded neutral density filter, tiled, flat panel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,579,031 (LIANG) 26 November 1996, abstract, figures 1-2, column 2, lines 60-67 and column 3, lines 1-39.	1
X --- Y	US, A, 5,396,257 (SOMEYA ET AL.) 07 March 1995, abstract, figure 1-2, column 1, lines 43-61, column 2, lines 51-62, column 24, lines 10-31.	1, 2, 5, 6 --- 3, 4, 7-13
Y	US, A, 5,046,827 (FROST ET AL.) 10 September 1991, abstract and figure 4a and 6a-b.	3, 4, 9, 10
Y	US, A, 5,105,183 (BECKMAN) 14 April 1992, abstract, figure 2 and column 1, lines 59-68.	1

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 22 MAY 1997	Date of mailing of the international search report 24 JUN 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer PAUL A. BELL Telephone No. (703) 306-3019

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/04869

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,982,275 (BRODY) 01 January 1991, abstract, figure 1, column 2, lines 43-47.	7-13
Y	US, A, 4,825,201 (WATANABE ET AL.) 25 April 1989, abstract, figures 5 and 7, column 1, lines 13-68.	1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/04869

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

345/1, 32, 88, 90, 102, 103, 150, 152, 153; 348/383, 791; 349/106, 109, 112